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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,733	07/12/2006	Takeshi Ichikawa	03500.109228	6040
	7590 11/17/200 CELLA HARPER &	EXAMINER		
30 ROCKEFELLER PLAZA			AHMED, SELIM U	
NEW YORK, NY 10112			ART UNIT	PAPER NUMBER
			2826	
			MAIL DATE	DELIVERY MODE
			11/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)			
	10/585,733	ICHIKAWA, TAKESHI			
Office Action Summary	Examiner	Art Unit			
	SELIM AHMED	2826			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period v - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	lely filed the mailing date of this communication. (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on 18 Se	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4) Claim(s) 1-16 is/are pending in the application. 4a) Of the above claim(s) 1-10 is/are withdrawr 5) Claim(s) is/are allowed. 6) Claim(s) 11-16 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or are subject to restriction and/or are subject to by the Examine 10) The specification is objected to by the Examine 10) The drawing(s) filed on 12 July 2006 is/are: a) Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct	r election requirement. r. ☐ accepted or b)☑ objected to be drawing(s) be held in abeyance. See ion is required if the drawing(s) is objected to be the drawing(s) is objected.	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).			
11) The oath or declaration is objected to by the Ex	anniler. Note the attached Office	Action of form F10-152.			
Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 07/12/2006, 10/3/2007.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ite			

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DETAILED ACTION

Election/Restrictions

 Applicants' election without traverse of Group II, including claims 11-16 in the reply filed on 09/18/2008 is acknowledged. Claims 1-10 are considered as non elected invention and withdrawn from examining consideration.

Information Disclosure Statement

 The Information Disclosure Statements has been filed on 07/12/2006, 10/03/2007 are considered.

Oath/Declaration

3. The oath or declaration filed on 07/12/2006 is acceptable.

Drawings

- 4. The drawings are objected to because of following informalities:
 - a. Features such as Vr1, Vsig1-Vr1, VFDsig1, Qsig etc outlined in para [0035-40] are not shown in the drawings.
 - Buried channel and surface channel MOS transistors are not labeled in the drawings.
 - c. Prior Art not labeled (Fig. 5).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

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Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto et al (US 2004/0263657; Sakamoto hereinafter).

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With regard to claim 11, Sakamoto discloses a method of manufacturing a semiconductor apparatus e.g. Figs. 5A, 5B provided with both a buried channel 68 type first conductive type (n-type) MOS transistor and a surface channel type 62 first conductive type (n-type) MOS transistor, wherein a first conductive type impurity region 65 is formed in channel positions of said buried channel type and surface channel type MOS transistors in the same step (Fig. 5A, region 65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 6,100,551; Lee hereinafter) in view of Sakamoto (US 2004/0263657).

With regard to claim 12, Lee discloses a method of manufacturing a solid state image pickup device e.g. Fig. 2 having a photoelectric conversion portion 12 and a pixel including a plurality of transistors (TX, RESET) formed in correspondence to said photoelectric conversion portion, in a substrate 2, wherein said plurality of transistors includes a buried channel type TX first

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conductive (n-type) type MOS transistor and a surface channel type (RESET) first conductive type (n-type) MOS transistor, and a first conductive type impurity region is formed in channel positions of said buried channel type and surface channel type MOS transistors.

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As discussed above, Lee discloses all of the limitations of claim 12 with the exception of a first conductive type impurity region is formed in channel positions of said buried channel type and surface channel type MOS transistors. However, in Figs. 5A, 5B of Sakamoto discloses a first conductive type impurity region 65 is formed in channel positions of said buried channel type and surface channel type MOS transistors. It would have been obvious to one having ordinary skill in the art at the time of the invention to include Sakamoto's first conductive type impurity region 65 in channel positions of said buried channel type and surface channel type MOS transistors for predictable result.

With regard to claim 15, e.g. in Figs 2, 4 of Lee (in view of Sakamoto) discloses a method of manufacturing a solid state image pickup device as claimed in any one of claims 12 to 14, wherein said first conductive type is of an n-type.

With regard to claim 16, Lee in view of Sakamoto discloses all of the limitations of claim 16 with the exception of an arsenic is used as a dopant of the first conductive type channel dope layer. It would have been obvious to one

having ordinary skill in the art at the time of the invention to use Arsenic as a ntype dopant for predictable result.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 6,100,551; Lee hereinafter) in view of Sakamoto (US 2004/0263657) and further in view of Watanabe (US 5880494).

With regard to claim 13, Lee in view of Sakamoto discloses all of the limitations of claim 12 but does not disclose a second conductive type impurity region is formed in the channel region of said surface channel type MOS transistor. However, in Fig. 27B of Watanabe discloses a second conductive type (p-type) impurity region 135 is formed in the channel region of said surface channel type MOS transistor. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Lee's (modified by Sakamoto) structure with a second conductive type (p-type) impurity region for predictable result.

With regard to claim 14, Watanabe (in view of Lee in view of Sakamoto) discloses a method of manufacturing a solid state image pickup device as claimed in claim 13, wherein a doze amount (n) of said first conductive type channel dope layer is smaller (n<p+) than a doze amount (p+) of said second conductive type channel dope layer. It would have been obvious to one having

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ordinary skill in the art at the time of the invention to choose specific amount of dose for optimizing electrical characteristic.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SA

/Evan Pert/

Primary Examiner, Art Unit 2826